Notice of Allowability	Application No.	Applicant(s)	
	10/067,038	YEH, TSE-YU	
	Examiner	Art Unit	
	Aimee J. Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *RCE and Amendment as received on 25 September 2006*.

2. ☒ The allowed claim(s) is/are *1, 2, 4, 5, 10-12, 14, 15, 18, 23-25 and 27 herein referred to as 1-14*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

2. Authorization for this examiner's amendment was given in a telephone interview with William Kid (Reg. No. 31,772) on 05 December 2006 and 12 December 2006.

3. The application has been amended as follows:

a. Claim 1: (Currently Amended) A processor comprising:

i. A queue configured to store one or more entries identifying a cache miss, the one or more entries including a destination register field to identify a destination register associated with the [[cash]]cache miss and a tag associated with each destination register field to identify a fill corresponding to a cache miss for an entry; and

ii. A control circuit coupled to the queue, wherein the control circuit is configured to detect a load miss of a load instruction in a load/store pipeline, the load/store pipeline being separate from an integer instruction pipeline and a separate floating point instruction pipeline, and wherein the control circuit is configured to enter into a stall state and inhibit issuance of instructions to the integer and floating point instruction pipelines to prevent replay of integer and floating point instructions dependent on the load miss, the control circuit to couple a destination register value to the

queue associated with the load miss, in which the queue is to respond with a fill tag associated with the destination register, the control circuit to store the fill tag in a miss tag register and to compare the fill tag in the miss tag register with fill tags of fill data being returned, wherein when a returned fill tag matches the fill tag in the miss tag register, the integer and floating point pipelines exit the stall state.

b. Claim 14: (Currently Amended) A method comprising:

i. Detecting a load miss of a load instruction in a load/store pipeline of a processor, the load/store pipeline being separate from an integer instruction pipeline and a separate floating point instruction pipeline;

ii. Comparing a destination register corresponding to the load instruction causing the load miss to other instructions in the queue for dependencies to the load miss;

iii. Inhibiting issuance of one or more instructions to the integer and floating point instruction pipelines responsive to detecting the load/miss in the load/store pipeline by entering a stall state to prevent replay of integer and floating point instructions;

iv. Sending a destination register value to a queue that stores an entry identifying the load miss, the entry including a destination register field to identify a destination register associated with the load miss and a tag associated with the destination register field of the load miss to identify a fill tag corresponding to the load miss;

v. Returning the fill tag from the queue as a miss tag;

vi. Storing the miss tag corresponding to the load miss in a register;

vii. Comparing a fill tag of fill data being returned to the miss tag to identify when fill data corresponding to the load miss is being returned; and

viii. Exiting the stall state to allow one or more instructions to issue to the integer and floating point instruction pipelines when a fill tag of fill data matches the miss tag.

c. Claim 27: Canceled

4. The following is an examiner's statement of reasons for allowance:

5. The independent claims essentially recite that the system has three pipelines: load, integer, and floating point. The load pipeline inhibits issuance of at least one instruction to the integer and floating point pipelines when a cache miss is detected until the cache miss is resolved via the use of tags to prevent replay of integer and floating point instructions dependent on the load miss. Prior art has not taught in a single reference system with three pipelines that inhibits issuance of dependent instructions to the integer and floating point pipelines until the cache miss is resolved. Prior art, including those cited in the attached PTO-892 Notice of Reference Cited, has taught in different patents and non-patent literature systems with separate and distinct load, integer, and floating point pipelines. However, these references either do not teach how a load cache miss is handled or teaches that speculative execution is present in the system. This means that the system would speculatively execute instructions dependent on the load instruction causing the cache miss. Consequently, the system must reissue, e.g. replay, the dependent instructions when the cache miss occurs. The prior art with multiple pipelines teaches that

delaying issuance of instructions dependent on the load instruction prevents the system from taking full advantage of the multiple pipelines, thereby teaching away from delaying dependent instructions, as in the claims. Prior art was also found that taught delaying instructions dependent on the load instruction causing the cache miss. However, these systems only have at most separate integer and floating point pipelines. The integer and floating point pipelines execute the load instructions within one of these pipelines, usually the integer. Therefore, the prior art lacks the third separate load/store pipeline that prohibits at least one instruction from issuing to a separate integer pipeline and a separate floating point pipeline. To combine one of the prior art references teaching multiple pipelines would be improper, since the prior art teaching delaying the instructions would essentially erase one of the primary benefits and motivations to using the multiple pipeline technique.

6. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:00am-4:30pm.

8. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

9. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AJL
Aimee J. Li
5 December 2006

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